

CCD 485 4096x4097

FULL FRAME IMAGE SENSOR



TECHNICAL SPECIFICATIONS

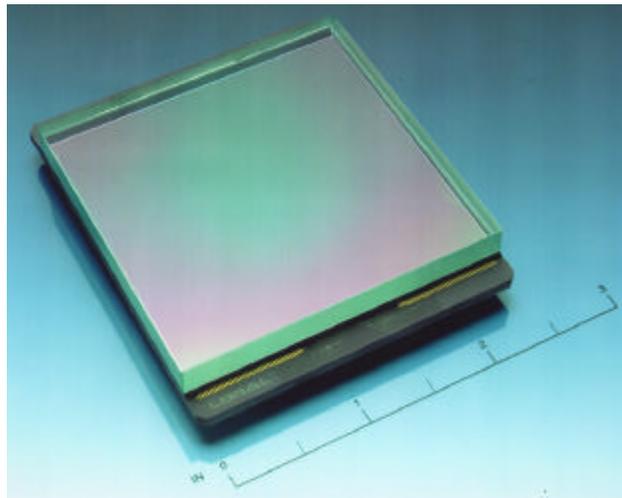
FOR

CCD485

APRIL 5, 1998

FEATURES

- 4096 x 4097 Photosite Array
- 15µm x 15µm Pixel Size
- 61.20 mm x 61.21 Active Image Area
- 4080 x 4081 Optically Active Pixels
- Near 100 % Fill Factor
- Multi-Pinned Phase (MPP) Option
- Low Readout Noise
- Wide Dynamic Range
- Three Phase Buried Channel NMOS



GENERAL DESCRIPTION

The CCD485 is a 4096 x 4097 element solid state Charge Coupled Device (CCD) Full Frame area image sensor which is intended for use in high resolution scientific, industrial, and commercial electro-optical systems. The CCD485 is organized as a matrix array of 4096 horizontal by 4097 vertical CCD photosites. The pixel pitch and spacing is 15µm.

The imaging array may be operated in one of two modes, Buried Channel or Multi-Pinned Phase (MPP). The Buried Channel operation offers low noise performance and excellent charge transfer efficiencies. An additional implant under one vertical phase creates a barrier which allows electrons to be collected under the other two phases. This mode, known as MPP, decreases dark current down to 25 pA/cm² @ 25°C. Excellent low noise performance is achieved by use of the buried channel CCD structure and a dual stage low noise output amplifier with an output conversion of 3µV/e.

Device processing is done using 2.5 micron design rules. The single metal, triple-poly process allows a photosite layout with small pixel geometries and few array blemishes.

FUNCTIONAL DESCRIPTION

The CCD485 consists of the following functional elements illustrated in the block diagram.

Image Sensing Elements: Incident photons pass through a transparent polycrystalline silicon gate structure creating electron hole pairs. The resulting

photo-electrons are collected in the photosites during the integration period. The amount of charge accumulated in each photosite is a linear function of the localized incident illumination intensity and integration period.

The photosite structure is made up of contiguous CCD elements with no voids or inactive areas. In addition to sensing light, these elements are used to shift image data vertically. Consequently, the device needs to be shuttered during readout.

Vertical Charge Shifting: The Full Frame architecture of the CCD485 provides video information as a single sequential readout of 4097 lines, each containing 4096 photosite elements. At the end of an integration period the ΦV_1 , and ΦV_2 , and ΦV_3 clocks are used to transfer charge vertically through the CCD array to the horizontal readout register. Vertical columns are separated by a channel stop region to prevent charge migration.

The imaging area is divided into four quadrants. Each quadrant may be clocked independently, if desired. The CCD485 may be clocked such that the full array is read out from any one of the four output amplifiers.

The last clocked gate in the Horizontal registers (ΦSG) is larger than the others and can be used to horizontally bin charge. This gate requires its own clock which should be tied to ΦH_1 for normal full resolution readout. The output video is available following the high to low transition of ΦSG .

Output Amplifier: The CCD485 has four output amplifiers. They are dual FET floating diffusion amplifiers with a reset MOSFET tied to the input gate. Charge packets are clocked to a precharged capacitor whose potential changes linearly in response to the number of electrons delivered. This potential is applied to the input gate of an NMOS amplifier producing a signal at the Output V_{OUT} pin. The capacitor is reset with ΦR to a precharge level prior to the arrival of the next charge packet except when horizontally binning. It is reset by use of the reset MOSFET. The output amplifier drain is tied to VDD. The source (Video Out) is connected to an external load resistor to ground. The source constitutes the video output from the device.

Multi-Pinned Phase: MPP is a CCD technology which significantly reduces the dark current generation rate. CCDs are endowed with this capability by the addition of an implant during the semiconductor manufacturing process.

This implant creates a barrier in the array which allows charge integration while maintaining pixel integrity with the Vertical clocks in the low state. Leaving the Vertical clocks in the low state during the integration cycle is the method used to implement MPP mode.

A drawback to utilizing the MPP mode is reduced full well capacity. The virtual well created by the MPP implant does not hold as much charge as the normal buried channel operating mode, which leaves one Vertical clock in the high state during integration. The CCD485 may be operated in the conventional buried channel mode with increase in charge capacity over the MPP mode.

DEFINITION OF TERMS

Charge-Coupled Device-A charge-coupled device is a monolithic silicon structure in which discrete packets of electron charge are transported from position to position by sequential clocking of an array of gates.

Vertical Transport Clocks $\phi V_1, \phi V_2, \phi V_3$ -The clock signals applied to the vertical transport register. 3 ϕ Vertical clocks are separated into 4 groups (A-D) for 12 ϕ clocking flexibility. This is utilized for color applications and integration time splitting.

Horizontal Transport Clocks $\phi H_1, \phi H_2, \phi H_3$ -The clock signals applied to the horizontal transport registers.

Reset Clock ϕR -The clock applied to the reset switch of the output amplifier.

Dynamic Range -The ratio of saturation output voltage to RMS noise in the dark. The peak-to-peak random noise is 4-6 times the RMS noise output.

Saturation Exposure -The minimum exposure level that produces an output signal corresponding to the maximum photosite charge capacity. Exposure is equal to the product of light intensity and integration time.

Responsivity -The output signal voltage per unit of exposure.

Spectral Response Range -The spectral band over which the response per unit of radiant power is more than 10% of the peak response.

Photo-Response Non-Uniformity -The difference of the response levels between the most and the least sensitive regions under uniform illumination (excluding blemished elements) expressed as a percentage of the average response.

Dark Signal -The output signal in the dark caused by thermally generated electrons. Dark signal is a linear function of integration time and an exponential function of chip temperature.

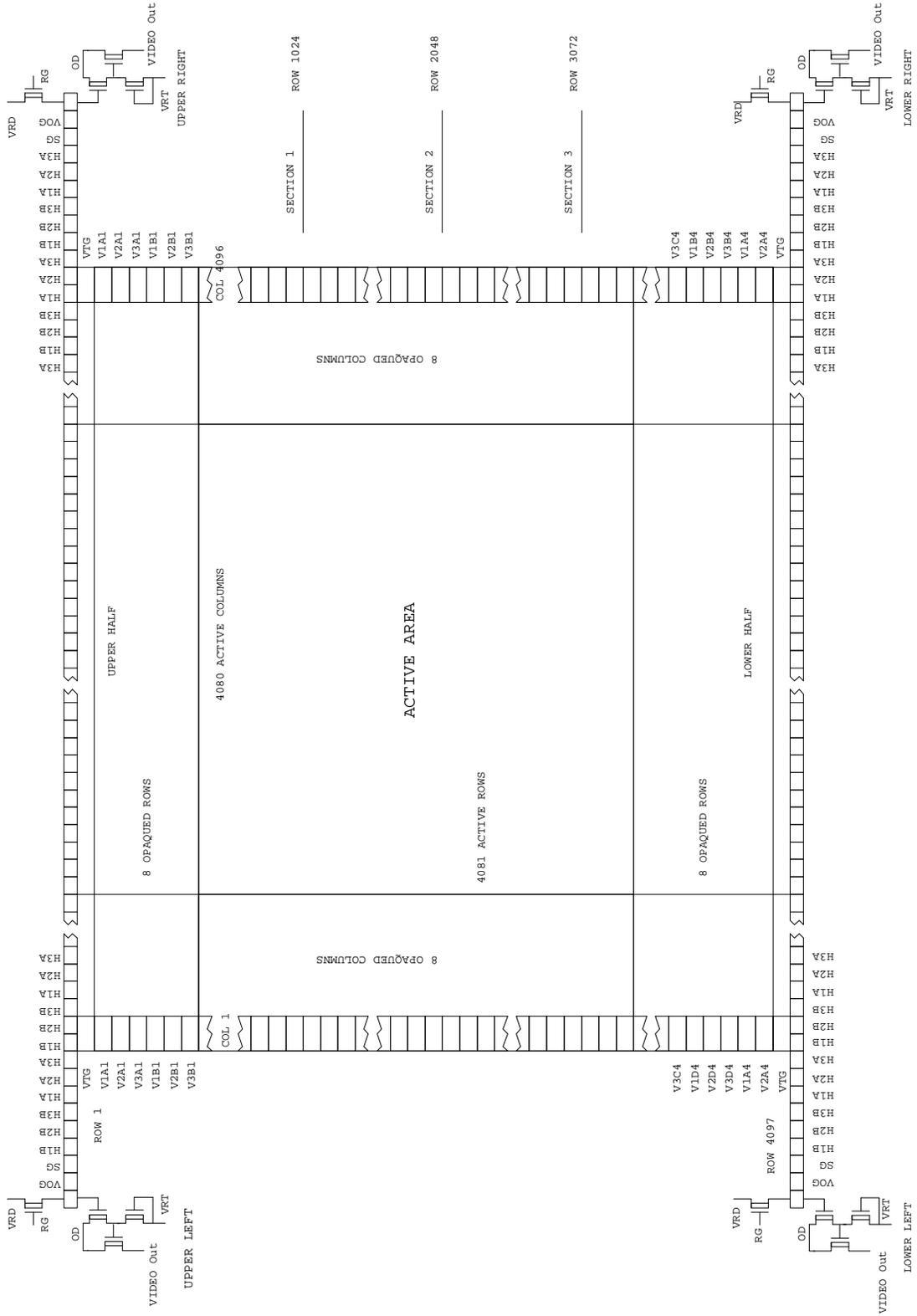
Vertical Transfer Gate ϕVTG - Gate structures adjacent to the end row of photosites and the horizontal transport registers. The charge packets accumulated in the photosites are shifted vertically through the array. Upon reaching the end row of photosites, the charge is transferred in parallel via the transfer gates to the horizontal transport shift registers whenever the transfer gate voltage goes low.

Pixel - Picture element or sensor element also called photoelement or photosite.

CCD 485 4096X4097 ELEMENT



FULL FRAME IMAGE SENSOR



PERFORMANCE CHARACTERISTICS: (MPP MODE) $T_p = 25^\circ\text{C}$ (Notes 1 & 2)						
SYMBOL	PARAMETER	RANGE			UNIT	CONDITION
		MIN	TYPICAL	MAX		
DS_{AVE}	Dark Signal, (Readout)		2.5	15	mV	Note 3
I_{DARK}	Dark Current Density (Integration)		25	100	pA/cm^2	Note 3
DSNU	Dark Signal Non-Uniformity		5	10	mV	Note 4
Q_{Sat}	Full Well Capacity	60	90		Ke^-	
V_{Sat}	Saturation Voltage	120	215		mV	
PRNU	Photoresponse Nonuniformity			10	% of V_{sat}	Note 5
CTE (V)	Charge Transfer Efficiency, Vertical	.99999	.999995		Per Phase Transfer	
CTE (H)	Charge Transfer Efficiency, Horizontal	.99995	.999995		Per Phase Transfer	
R	Responsivity		1.0		$\text{V}/\mu\text{J}/\text{cm}^2$	
S_{SF}	Sensitivity (Scale Factor)	2.0	2.5		$\mu\text{V}/\text{e}^-$	

PERFORMANCE CHARACTERISTICS: (NON-MPP MODE) $T_p = 25^\circ\text{C}$ (Note 1 & 2)						
SYMBOL	PARAMETER	RANGE			UNIT	CONDITION
		MIN	TYPICAL	MAX		
I_{DARK}	Dark Current Density		2		nA/cm^2	Note 3
Q_{Sat}	Full Well Capacity		400		Ke^-	
V_{Sat}	Saturation Voltage		1,000		mV	

DC CHARACTERISTICS: $T_p = 25\text{ }^\circ\text{C}$ (Note 1)						
SYMBOL	PARAMETER	RANGE			UNIT	CONDITION
		MIN	TYPICAL	MAX		
V_{DD}	DC Supply Voltage	17	20	23	Volts	
V_{RD}	Reset Drain Voltage	12	14	16	Volts	
V_{OG}	Output Gate Voltage	0	1	5	Volts	
V_{SS}	Substrate Ground	0	0	0	Volts	
V_{RT}	Output Amplifier Return	0	3	5	Volts	

CLOCK CHARACTERISTICS: (MPP MODE) $T_p = 25\text{ }^\circ\text{C}$ (Note 1)						
SYMBOL	PARAMETER	RANGE			UNIT	CONDITION
		MIN	TYPICAL	MAX		
$V_{\phi H(1,2,3)}$ HIGH	Horizontal Transport Clock HIGH	+ 2	+ 5	+ 8	Volts	
$V_{\phi H(1,2,3)}$ LOW	Horizontal Transport Clock LOW	- 8	- 5	0	Volts	
$V_{\phi SG}$ HIGH	Summing Gate Clock HIGH	+ 2	+ 5	+ 8	Volts	
$V_{\phi SG}$ LOW	Summing Gate Clock LOW	- 8	- 5	0	Volts	
$V_{\phi V(1,2,3)}$ HIGH	Vertical Transport Clocks HIGH	0	+ 3	+ 6	Volts	
$V_{\phi V(1,2,3)}$ LOW	Vertical Transport Clocks LOW	- 10	- 8	- 5	Volts	
$V_{\phi R}$ HIGH	Reset Gate Clock HIGH	+ 6	+ 10	+ 14	Volts	
$V_{\phi R}$ LOW	Reset Gate Clock LOW	- 4	0	+ 2	Volts	
$V_{\phi VTG}$ HIGH	Vertical Transfer Gate Clock HIGH	0	+ 3	+ 6	Volts	
$V_{\phi VTG}$ LOW	Vertical Transfer Gate Clock LOW	- 10	- 8	- 5	Volts	

CLOCK CHARACTERISTICS: (NON-MPP MODE) $T_p = 25\text{ }^\circ\text{C}$ (Note 1)						
SYMBOL	PARAMETER	RANGE			UNIT	CONDITION
		MIN	TYPICAL	MAX		
$V_{\phi H(1,2,3)}$ HIGH	Horizontal Transport Clock HIGH	2	+ 5	+ 8	Volts	
$V_{\phi H(1,2,3)}$ LOW	Horizontal Transport Clock LOW	- 8	- 5	0	Volts	
$V_{\phi V(1,2,3)}$ HIGH	Vertical Transport Clocks HIGH	+ 5	+ 9	+ 15	Volts	
$V_{\phi V(1,2,3)}$ LOW	Vertical Transport Clocks LOW	- 2	0	+ 4	Volts	
$V_{\phi R}$ HIGH	Reset Gate Clock HIGH	+ 6	+ 10	+ 14	Volts	
$V_{\phi R}$ LOW	Reset Gate Clock LOW	- 4	0	+ 2	Volts	
$V_{\phi VTG}$ HIGH	Vertical Transfer Gate Clock HIGH	+ 5	+ 9	+ 15	Volts	
$V_{\phi VTG}$ LOW	Vertical Transfer Gate Clock LOW	- 2	0	+ 4	Volts	

AC CHARACTERISTICS: $T_p = 25\text{ }^\circ\text{C}$ (Note 1)						
SYMBOL	PARAMETER	RANGE			UNIT	CONDITION
		MIN	TYPICAL	MAX		
V_{ODC}	Output DC Level	13	16.4	19	Volts	Note 6
R_o	Output load Resistor	1.0	5.0	20	$K\Omega$	
$f_{MAX\text{ HORIZ.}}$	Horizontal Clock Frequency		5	10	MHz	
P_D	On-Chip Power Dissipation		1.0		W	Note 7

CCD 485 4096x4097 CHARACTERISTIC NOTES



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NOTES

- 1.- T_p is defined as the package temperature.
- 2.- Standard test conditions are nominal MPP clocks and DC operation voltages. 5.2 MHz horizontal data rate, integration time = 5.25 msec. Values shown are for 25 °C, unless otherwise indicated.
- 3.- Dark Current doubles every 5-7 °C.
- 4.- Excluding spikes.
- 5.- Excluding spikes, and measured @ $\frac{1}{2}V_{sat}$
- 6.- For the cases of $V_{RD} = \text{MIN, TYPICAL, MAX}$ and $R_o = 5 \text{ k}\Omega$
- 7.- At $f_{MAX} = 5 \text{ MHz}$, one On-Chip amplifier output, vertical & horizontal registers.
- 8.- Device has 4 On-Chip amplifier output options.

COSMETIC SPECIFICATION Maximum Allowable in:	COSMETIC GRADING CCD 485		
	1	2	3
CENTRAL REGION			
Value of X & Y	3	5	10
Defective Columns > 1 x Y pixels (Total)	12	24	40
Defective Rows > X x 1 pixels (Total)	12	24	40
Maximum Defective Cluster Size (X x Y)	3 x 3	5 x 5	10 x 10
Defective Pixels (including Clusters, but excluding Col/Row defects)	400	600	1,200
Maximum Adjacent Defective Columns/Rows	3	4	5
Minimum number of good pixels between occurrences	4	4	2
OUTSIDE CENTRAL REGION			
Value of X & Y	3	5	10
Defective Columns > 1 x Y pixels (Total)	20	45	70
Defective Rows > X x 1 pixels (Total)	20	45	70
Maximum Defective Clusters Size	3 x 3	5 x 5	10 x 10
Defective Pixels, (including Clusters, but excluding Col/Row defects)	1,600	2,400	4,800
Maximum Adjacent Defective Columns/Rows	3	4	5
Adjacent Defective Columns/Rows per single occurrence	0	5	6,7,8,9,10
Minimum number of good pixels between occurrences	4	4	2
NOTES			
<p>1.- Cosmetic testing is done under uniform illumination . It is typically measured under ½ Vsat illumination. Consult Lockheed Martin Fairchild Systems for Custom Selections.</p> <p>2.- Total number of clusters must contain ≤ the number of defective pixels allowed.</p>			

COSMETICS SPECIFICATIONS

DEFINITIONS:

Adjacent.- Neighboring and touching.

Active Pixel.- A pixel that is responsive to light or energy.

Central Zone.- The centered area of the total imaging area. For example, for CCD442A (2048 x 2048 pixels), the centered 1K x 1K coordinates are: $\{512 \leq (x, y) \leq 1512\}$. For a CCD485 & CCD481 (4096x4096 pixels), the centered 2K x 2K coordinates are: $\{1024 \leq (x, y) \leq 3072\}$.

Cluster.- A group of defective pixels.

Cluster Size: The area enclosing the group of defective pixels. The area dimensions are specified by the Cartesian coordinates of X x Y pixels. The length and width of "X & Y" are given in the *Cosmetic Specification* table for a specified device grade.

Column.- Any > 1 x Y consecutive pixels. The length of "Y" is given in the *Cosmetic Specification* table for a given device grade. Therefore, a section larger than 1 x Y in the vertical direction (following Cartesian coordinates) is considered a column. If smaller than 1 x Y, it is considered as a cluster.

Dead Pixel.- A pixel that fails to respond to light or energy.

Inactive Pixel.- A pixel that is not responsive to light or energy by design, such as dark reference pixels.

Outer Zone.- The area outside the central zone. For example: For CCD442A the outside surrounding a centered 1K x 1K coordinates are: $\{1 \leq (x, y) < 512\}$ & $\{1512 < (x, y) \leq 2048\}$. For CCD485 & CCD481 (4096 x 4096 pixels), the outside surrounding a centered 2K x 2K coordinates are: $\{1 \leq (x, y) < 1024\}$ & $\{3072 < (x, y) \leq 4096\}$.

Pixel.- One picture element of an imaging array.

Row.- Any > X x 1 consecutive pixels. The length of "X" is given in the *Cosmetic Specification* table for a given device grade. Therefore, a section larger than X x 1 in the horizontal direction (following Cartesian coordinates) it is considered a row. If smaller than X x 1, it is considered a cluster.

TYPE OF COSMETIC DEFECTS

Bright Columns/Rows/Clusters: Any Column/Row/Cluster that fails the PRNU specification and is *brighter* then the local average signal.

Column Shifts: A column (or group of columns) in which some or all of the pixels appear shifted up or down with respect to its adjacent columns. This phenomena is also known as “weeping”. Column shifts are treated as defective columns.

Dark Columns/Rows/Clusters: Any Column/Row/Cluster that fails the PRNU specification and is *darker* then the local average signal.

Defective Pixel: Any pixel which fails the PRNU specification.

Defective Column: Any >1x Y consecutive defective pixels. The length of “Y” is given in the *Cosmetic Specification* table for a given device grade.

Defective Rows: Any > X x 1 consecutive defective pixels. The length of “X” is given in the *Cosmetic Specification* table for a given device grade .

Defective Cluster: Any group of defective pixels in which one or more pixels are contained outside the specified cluster size. Below is an example of a cluster rejected for a maximum cluster size of a 10 x 10 pixels size.

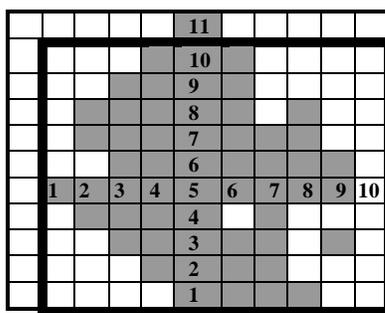


Fig. 1 Example of a defective 9 x 11 Cluster.

(this cluster will fail a maximum cluster size spec of 10 x 10 since one pixel extends outside the X x Y specified area. Total Bad Pixels = 56)

FOR INFORMATION ONLY:

Proximity Pixel/Col/Row/.- Correctable Pixel/Row/Col/defects that fall within the unallowable proximity to the next defect. (i.e. bad columns/rows that do not have the minimum distance allowable for the next defect, but they can be corrected and agree in quantity with the specification). For example, the minimum spacing allowed between defects is 5 pixels. Therefore if you have 2 bad columns separated by one good, it will fail if your spec allows you to have only 2 adjacent defective columns. Thus, it does not meet the spacing criteria. This example would be a “proximity 2 columns” and not adjacent 2 columns).

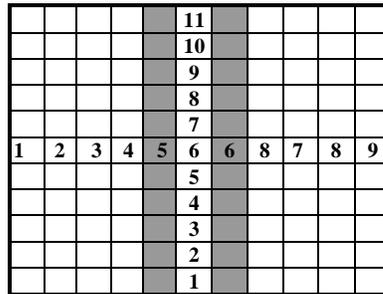


Fig. 1 Example of proximity 2 columns.

Stair Case Cluster: Pixels that fall outside the cluster size (X x Y), but have $\leq X \times Y$ number of allowable bad pixels. The following examples illustrates its advantages.

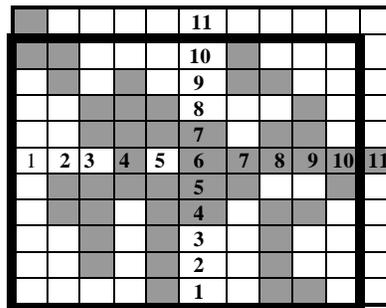


Fig. 2 Example of a Stair Case Cluster.

(this cluster would be rejected since two pixels extends outside the X x Y area : Total Bad Pixels = 47)

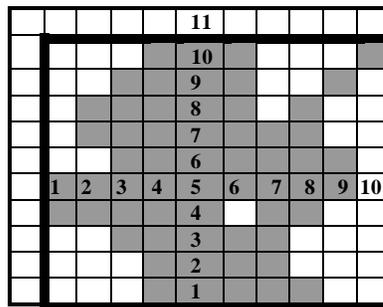
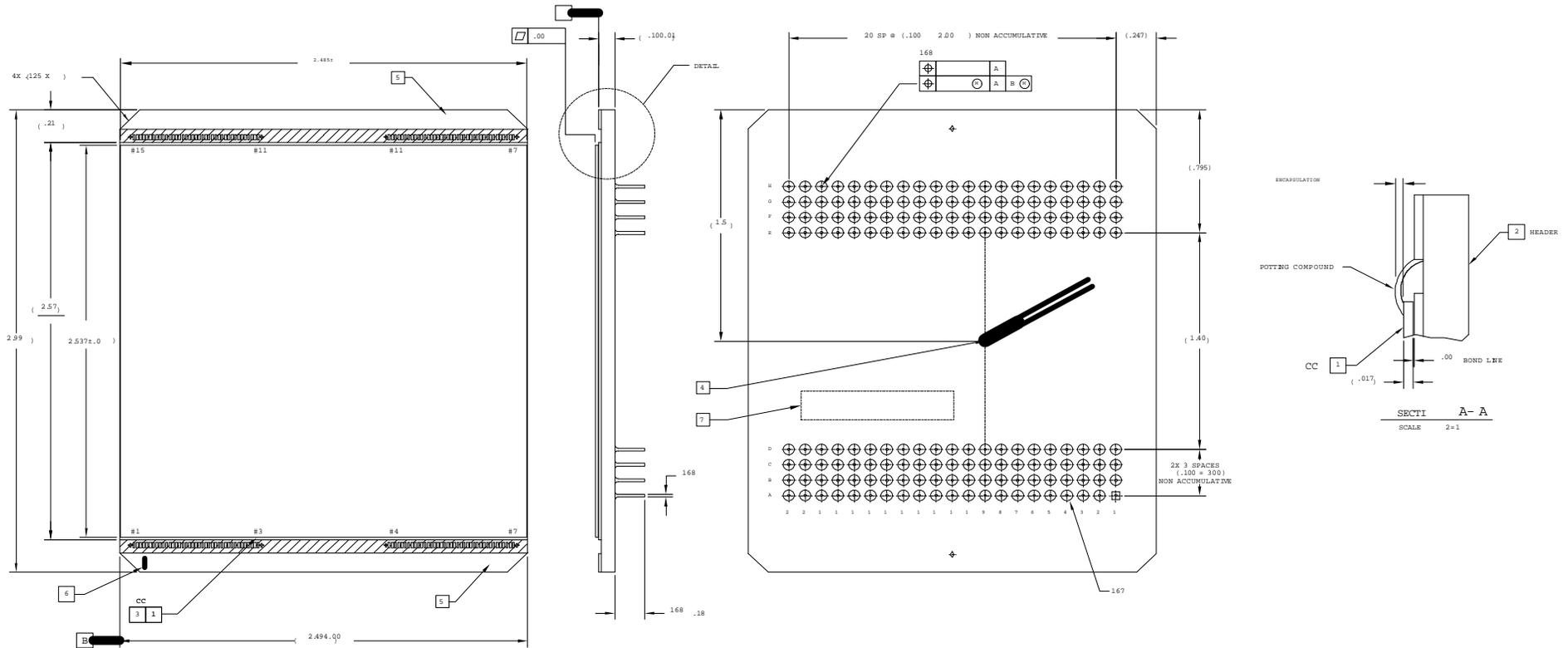


Fig. 3 Example of a Defective Cluster.

(this cluster would pass spec since no pixels extends outside the X x Y area : Total Bad Pixels = 59).

CCD 485 4096X4097 PACKAGING SPECIFICATION

FULL FRAME IMAGE SENSOR

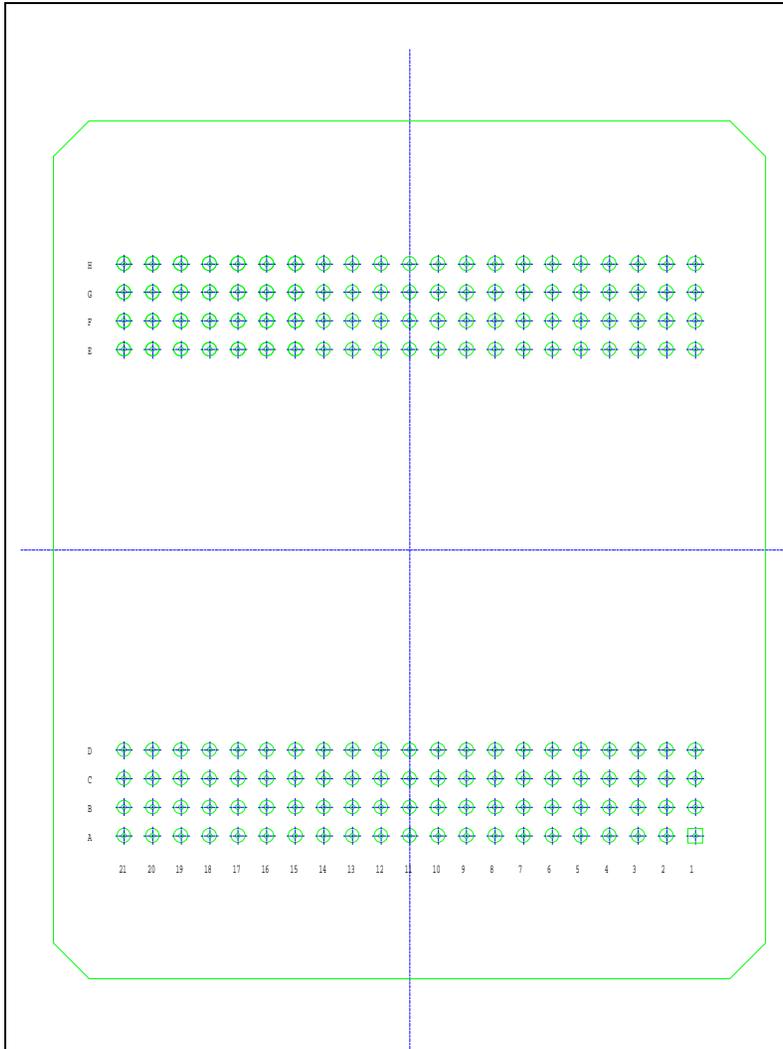


NOTES:	
① FOCAL PLANE ARRAY (CCD485)	
② HEADER	
③ CCD SHALL NOT OVERHANG SIDES OF HEADER	
④ TEMP SENSOR (OPTIONAL)	
⑤ SLIGHT CHIPPING US ALLOWED IN THIS AREA AS LONG AS FUNCTIONALITY IS UNAFFECTED	
⑥ MARK ARROW IS APPROXIMATE POSITION SHOWN TO INDICATE PIN # 1	
⑦ DEVICE IDENTIFICATION NUMBER (APPROXIMATE LOCATION)	
PACKAGING	ALUMINA TRIOXIDE (AL ₂ O ₃) PIN GRID ARRAY (PGA)
PIN LENGTH	0.180" ± 0.020"

CCD 485 4096X4097 PACKAGE PINOUT SPECIFICATION



FULL FRAME IMAGE SENSOR



CCD485 PINOUT								
	A	B	C	D	E	F	G	H
1	VDD _{UL}	VOG _{UL}	H1 _{UL}	H1 _{UL}	H1 _{UR}	H1 _{UR}	VOG _{UR}	VDD _{UR}
2	Vout _{UL}	φSG _{UL}	H3 _{UL}	H2 _{UL}	H2 _{UR}	H3 _{UR}	φSG _{UR}	Vout _{UR}
3	VRT _{UL}	H3 _{UL}	H2 _{UL}			H2 _{UR}	H3 _{UR}	VRT _{UR}
4	VRD _{UL}	φR _{UL}	φVTG _{UL}	Vss	Vss	φVTG _{UR}	φR _{UR}	VRD _{UR}
5	V1 _{UH}	V2 _{UH}	V3 _{UH}	V1 _{UH}	V1 _{UH}	V3 _{UH}	V2 _{UH}	V1 _{UH}
6	V2 _{UH}	V3 _{UH}	V1 _{UH}	V2 _{UH}	V2 _{UH}	V1 _{UH}	V3 _{UH}	V2 _{UH}
7	V3 _{UH}	V1 _{UH}	V2 _{UH}	V3 _{UH}	V3 _{UH}	V2 _{UH}	V1 _{UH}	V3 _{UH}
8	V2 _{UH}	V3 _{UH}	V1 _{UH}	V3 _{UH}	V3 _{UH}	V1 _{UH}	V3 _{UH}	V2 _{UH}
9	V2 _{UH}	V1 _{UH}	V3 _{UH}	V2 _{UH}	V2 _{UH}	V3 _{UH}	V1 _{UH}	V2 _{UH}
10	V1 _{UH}	V3 _{UH}	V2 _{UH}	V1 _{UH}	V1 _{UH}	V2 _{UH}	V3 _{UH}	V1 _{UH}
11	Vss	Vss	Vss	Vss	Vss	Vss	Vss	Vss
12	V3 _{LH}	V1 _{LH}	V2 _{LH}	V3 _{LH}	V3 _{LH}	V2 _{LH}	V1 _{LH}	V3 _{LH}
13	V2 _{LH}	V3 _{LH}	V1 _{LH}	V2 _{LH}	V2 _{LH}	V1 _{LH}	V3 _{LH}	V2 _{LH}
14	V2 _{LH}	V1 _{LH}	V3 _{LH}	V1 _{LH}	V1 _{LH}	V3 _{LH}	V1 _{LH}	V2 _{LH}
15	V1 _{LH}	V3 _{LH}	V2 _{LH}	V1 _{LH}	V1 _{LH}	V2 _{LH}	V3 _{LH}	V1 _{LH}
16	V2 _{LH}	V1 _{LH}	V3 _{LH}	V2 _{LH}	V2 _{LH}	V3 _{LH}	V1 _{LH}	V2 _{LH}
17	V3 _{LH}	V2 _{LH}	V1 _{LH}	V3 _{LH}	V3 _{LH}	V1 _{LH}	V2 _{LH}	V3 _{LH}
18	VRD _{LL}	φR _{LL}	φVTG _{LL}	Vss	Vss	φVTG _{LR}	φR _{LR}	VRD _{LR}
19	VRT _{LL}	H3 _{LL}	H2 _{LL}			H2 _{LR}	H3 _{LR}	VRT _{LR}
20	Vout _{LL}	φSG _{LL}	H3 _{LL}	H2 _{LL}	H2 _{LR}	H3 _{LR}	φSG _{LR}	Vout _{LR}
21	VDD _{LL}	VOG _{LL}	H1 _{LL}	H1 _{LL}	H1 _{LR}	H1 _{LR}	VOG _{LR}	VDD _{LR}

UL = Upper Left UR = Upper Right UH = Upper Half
 LL = Lower Left LR = Lower Right LH = Lower Half